

A1
cont.

10. (Amended) A process according to any one of Claims 1-5, 7, or 8, wherein the floating gates are self-aligned to the third gates.

A2

24. (Amended) A process for producing a semiconductor integrated circuit device according to any one of claims 19-21 or 23, wherein the polycrystalline silicon film has a film thickness thinner than that of the first pattern which becomes the floating gates.

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32. (Amended) A process for producing a semiconductor integrated circuit device according to any one of claims 14-21, 23, or 25-31, wherein the third gates are formed as self-aligned to the floating gates.

33. (Amended) A process for producing a semiconductor integrated circuit device according to any one of claims 14-21, 23, or 25-31, wherein the floating gates are formed as self-aligned to the third gates.

Please add the following claims:

A4

40. (New) A process according to claim 6, wherein the third gates are self-aligned to the floating gates.

41. (New) A process according to claim 6, wherein the floating gates are self-aligned to the third gates.

A4
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42. (New) A process for producing a semiconductor integrated circuit device according to claim 22, wherein the polycrystalline silicon film has a film thickness thinner than that of the first pattern which becomes the floating gates.

43. (New) A process for producing a semiconductor integrated circuit device according to claim 22, wherein the third gates are formed as self-aligned to the floating gates.

44. (New) A process for producing a semiconductor integrated circuit device according to claim 22, wherein the floating gates are formed as self-aligned to the third gates.

45. (New) A process for producing a semiconductor integrated circuit device according to claim 24, wherein the third gates are formed as self-aligned to the floating gates.
